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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/556,779	04/25/2000	Seong-Hwan Moon	AB-1600 US	8043

32605 7590 06/03/2009

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EXAMINER	
KUMAR, SRILAKSHMI K	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
06/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/556,779	MOON ET AL.	
	Examiner	Art Unit	
	SRILAKSHMI K. KUMAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *March 4, 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14,17-21,23 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,17-21,23 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The following is in response to the Amendment filed March 4, 2009. Claims 1, 9 and 14 have been amended. Claims 13, 15, 16, 22, 24 and 25 have been cancelled. Claims 1-12, 14, 17-21, 23, 26-29 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-12, 20 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita et al (US 6,388,651) in view of Kim et al (US 6,229,516) and further in view of Hurokawa et al (US 6,054,975).

As to independent claim 1, Kinoshita et al disclose in Figs. 1-4, a liquid crystal display (1) comprising, a signal processor (Fig. 3, item G/A) for generating and outputting a first image

signal that corresponds to a portion of an image (col. 3, line 53-col. 4, line 41), and a second image signal that corresponds to a remaining portion of the image (out of the left and right of G/A, col. 3, line 53-col. 4, line 41), a driving control signal using an image data (into 701b-708b)), a main control signal (into G/A), the driving control signal including a source driving control signal including a source driving control signal and a gate driving control signal (col. 1, line 64-col. 2, line 12);

Kinoshita et al do not explicitly teach a power source all of which are supplied from an image supplying source. It would have been obvious to one of ordinary skill in the art that a power source is present as it is required in order for the liquid crystal display to operate.

Kinoshita et al teach a data signal driver for generating and outputting a data signal (out of 701b-708b) from the first image signal and the second image signal, the gray scale voltage and the source driving control signal all of which are input from said signal processor;

Kinoshita et al teach a printed circuit board having a plurality of wires for transmitting the signals and/or voltages of said signal processor to the data signal driver (Fig. 6, col. 1, line 64-col. 2, line 12);

Kinoshita et al teach a gate signal driver for generating and outputting a gate signal from the gate voltage and the gate driving control signal of said signal processor (col. 2, lines 55-64);

Kinoshita et al teach a liquid crystal display panel (100) for displaying an image formed by receiving the data signal from said data signal driver and the gate signal from said gate signal driver (col. 2, lines 55-64);

Kinoshita et al teach wherein the plurality of wires comprises a first group of wires for transmitting the first image signal and a second group of wires for transmitting the second image signal (Fig. 3, a plurality of wires grouped on the left and on the right of G/A), and the first

group of wires are entirely spaced apart from the second group of wires (col. 1, line 64-col. 2, line 12, col. 3, lines 7-27));

Kinoshita et al teach wherein the data signal driver includes two groups of the data signal driver outputting a data signal from the first and the second image signal, one of which the let side of the signal processor and the other which is the right side of the processor (Fig. 3, col. 3, lines 7-27).

Kinoshita et al fail to disclose where the first image signal and second image signal are simultaneously output. Kim et al teach in Fig. 3 an LCD with two groups of data, upper and lower. In Fig. 8, lines 6-28, Kim et al teaches the driving waveform that drives upper data and lower data at the same time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include where the first image signal and second image signal are simultaneously output as taught by Kim et al into that of Kinoshita et al as Kim improves the high quality of the image being displayed (col. 9, lines 60-67 of Kim).

Kinoshita et al as modified by Kim et al do not teach wherein edges of the printed circuit board and the signal processor are overlapped with each other and the overlapped portion of the printed circuit board and the signal processor is narrower than the remaining portion of the printed circuit board.

Hurokawa et al teach in Fig. 3, the overlapped portion (L2) of the printed circuit board (204) and the signal processor (301) has a narrower width than a remaining portion (L1) of the printed circuit board (204). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein edges of the printed circuit board and the signal processor are overlapped with each other and the overlapped portion of the printed circuit board and the signal processor is narrower than the remaining portion of the printed circuit board as

taught by Hurokawa et al into Kinoshita et al as modified by Kim et al as it is a predictable modification. This feature of Hurokawa et al provides technology which allows the distance between the input and output terminals to be reduced and to prevent the protecting film to be formed around the semiconductor chip from leaking to the areas of input and output terminals in a liquid crystal driving device.

As to independent claim 9, limitations of claim 1, and further comprising, Kinoshita et al disclose wherein the data signal driver comprises at least four source drive integrated circuits and is physically, electrically connected to said liquid crystal display panel by a connecting member mounting the source drive integrated circuits one to one (Fig. 3, col. 1, line 64-col. 2, line 28, col. 3, lines 7-27), wherein the connecting member includes a first group of connecting member and a second group connecting member, the first group of connecting member being connected with the first group of wires and the second group connecting member being connected with the second group of wires (Fig. 3, col. 1, line 64-col. 2, line 28, col. 3, lines 7-27).

Kinoshita et al do not disclose where the first image signal and second image signal are simultaneously output. Kim et al teach in Fig. 3 an LCD with two groups of data, upper and lower. In Fig. 8, lines 6-28, Kim et al teaches the driving waveform that drives upper data and lower data at the same time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include where the first image signal and second image signal are simultaneously output as taught by Kim et al into that of Kinoshita et al as Kim improves the high quality of the image being displayed (col. 9, lines 60-67 of Kim).

As to dependent claim 2, limitations of claim 1, and further comprising, Kinoshita et al disclose wherein the data signal driver comprises at least four source drive integrated circuits and is physically, electrically connected to said liquid crystal display panel by a connecting member

mounting the source drive integrated circuits one to one (Fig. 3, col. 1, line 64-col. 2, line 28, col. 3, lines 7-27), wherein the connecting member includes a first group of connecting member and a second group connecting member, the first group of connecting member being connected with the first group of wires and the second group connecting member being connected with the second group of wires (Fig. 3, col. 1, line 64-col. 2, line 28, col. 3, lines 7-27).

As to dependent claims 3 and 10, limitations of claims 2 and 9, and further comprising, Kinoshita et al disclose wherein the first image signal includes a first clock signal (Fig. 3, item LCK-L) and the second image signal includes a second clock signal (Fig. 3, item LCK-R), and the first clock signal and the second clock signal have a frequency half of a clock signal frequency supplied from the image supplying source (col. 5, lines 3-50)

As to dependent claims 4 and 11, limitations of claims 2 and 9, and further comprising, Kinoshita et al disclose wherein the first image signal includes a first shift signal and the second image signal includes a second shift signal, the first and second shift signals being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits have the same phase (col. 4, lines 8-24).

As to dependent claim 5, limitations of claim 2, and further comprising, Kinoshita et al disclose wherein the first image signal includes a first drive signal and the second image signal includes a second drive signal, the first and second drive signals being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits have the same phase (col. 3, lines 7-27).

As to dependent claims 6 and 12, limitations of claims 2 and 9, and further comprising, Kinoshita et al disclose wherein the first group of wires and the second group of wires are branched from a wire aggregation including a plurality of wires at a selected position (Figs. 3 and 4).

As to dependent claim 7, limitations of claim 1, and further comprising, Kinoshita et al disclose wherein said printed circuit board is a source printed circuit board.

As to dependent claim 8, limitations of claim 1, and further comprising, Kinoshita et al disclose wherein the first group of wires and the second group of wires are arranged in a T-shape on said printed circuit board (Figs. 3 and 5).

As to dependent claims 20 and 28, limitations of claims 1 and 9, and further comprising, Kinoshita et al disclose wherein the first and second image signals comprises a first clock signal and a second clock signal (Fig. 3, items LCK-L and LCK-R are the two clock signals), respectively, and the first and second clock signals have the same phase and frequency with each other (Fig. 4).

4. Claims 14, 17-19, 21, 23, 26, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita et al in view of Kim et al and Hurokawa et al (US 6,054,975)as applied to claims 1-12, 20 and 28 and further in view of Asada et al (US 5,963,287).

As to dependent claims 14 and 23, limitations of claims 13 and 22, and further comprising, Kinoshita et al and Kim et al do not disclose wherein an anisotropic conductive film is interposed between the overlapped edges of the printed circuit board and the signal processor. Asada et al disclose in col. 6, lines 12-15 wherein an anisotropic conductive film is interposed between the overlapped edges. It would have been obvious to one of ordinary skill in the art to include the configuration of the printed circuit board and signal processor and the anisotropic

conductive film as shown by Asada et al into Kinoshita et al as Asada et al disclose in col. 3, lines 28-35 and col. 4, lines 14-24 as this configuration would minimize bumps and the display unit may be manufactured inexpensively and with a high yield.

As to dependent claims 17 and 26, limitations of claim 1 and 9, and further comprising, Kinoshita et al and Kim et al do not disclose wherein the printed circuit board comprises a plurality of parts. Asada et al disclose in Fig. 3 wherein the printed circuit board comprises a plurality of parts. It would have been obvious to one of ordinary skill in the art to include the configuration of the printed circuit board and the plurality of parts as shown by Asada et al into Kinoshita et al as Asada et al disclose in col. 3, lines 28-35 and col. 4, lines 14-24 as this configuration would minimize bumps and the display unit may be manufactured inexpensively and with a high yield, and the plurality of parts are required for the operation of the liquid crystal display.

As to dependent claims 18 and 27, limitations of claims 17 and 26, and further comprising, Kinoshita et al and Kim et al do not disclose wherein the parts comprises a voltage supplying part, a gate voltage generating part, a gray scale voltage generating part and a timing controller. Asada et al disclose in col. 17, lines 62-67 wherein the parts comprises a voltage supplying part, a gate voltage generating part, a gray scale voltage generating part and a timing controller which are part of the control driver. It would have been obvious to one of ordinary skill in the art to include the configuration of the printed circuit board and the plurality of parts as shown by Asada et al into Kinoshita et al as Asada et al disclose in col. 3, lines 28-35 and col. 4, lines 14-24 as this configuration would minimize bumps and the display unit may be manufactured inexpensively and with a high yield, and the plurality of parts are required for the operation of the liquid crystal display.

As to dependent claim 19, limitations of claim 1, and further comprising, Kinoshita et al and Kim et al do not disclose wherein the printed circuit board is formed on a different substrate from a thin film transistor substrate of the liquid crystal display panel. Asada et al disclose wherein the printed circuit board is formed on a different substrate from the thin film transistor substrate of the liquid crystal display panel in col. 5, lines 55-67. It would have been obvious to one of ordinary skill in the art to include the configuration of the printed circuit board as shown by Asada et al into Kinoshita et al as Asada et al disclose in col. 3, lines 28-35 and col. 4, lines 14-24 as this configuration would minimize bumps and the display unit may be manufactured inexpensively and with a high yield.

As to dependent claims 21 and 29, limitations of claims 1 and 9, and further comprising, Kinoshita et al and Kim et al do not disclose wherein the wires are formed on one surface of the printed circuit board. Asada et al disclose wherein the wires are formed on one surface of the printed circuit board in Fig. 1, col. 1, lines 21-35. It would have been obvious to one of ordinary skill in the art to include the configuration of the printed circuit board as shown by Asada et al into Kinoshita et al as Asada et al disclose in col. 3, lines 28-35 and col. 4, lines 14-24 as this configuration would minimize bumps and the display unit may be manufactured inexpensively and with a high yield.

Response to Arguments

5. Applicant's arguments with respect to claims 1-12, 14, 17-21, 23, 26-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SRILAKSHMI K. KUMAR whose telephone number is (571)272-7769. The examiner can normally be reached on 7:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Srilakshmi K Kumar/
Primary Examiner
Art Unit 2629

SKK
June 1, 2009